DATA SHEET

74HC595; 74HCT595

8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

Product specification
Supersedes data of 1998 Jun 04

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Philips
Semiconductors

PHILIPS

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74HC595; 74HCT595

FEATURES

- 8-bit serial input
- 8-bit serial or parallel output
- Storage register with 3-state outputs
- Shift register with direct clear
- 100 MHz (typical) shift out frequency
- ESD protection:
  HBM EIA/JESD22-A114-A exceeds 2000 V
  MM EIA/JESD22-A115-A exceeds 200 V.

APPLICATIONS

- Serial-to-parallel data conversion
- Remote control holding register.

DESCRIPTION

The 74HC/HCT595 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT595 is an 8-stage serial shift register with a storage register and 3-state outputs. The shift register and storage register have separate clocks.

Data is shifted on the positive-going transitions of the SH_CP input. The data in each register is transferred to the storage register on a positive-going transition of the ST_CP input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register.

The shift register has a serial input (DS) and a serial standard output (Q7') for cascading. It is also provided with asynchronous reset (active LOW) for all 8 shift register stages. The storage register has 8 parallel 3-state bus driver outputs. Data in the storage register appears at the output whenever the output enable input (OE) is LOW.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			74HC	74HCT	
t_{PHL}/t_{PLH}	propagation delay	C_L = 50 pF; V_{CC} = 4.5 V			
	SH_CP to Q7'		19	25	ns
	SH_CP to Qn		20	24	ns
	$\overline{MR}$ to Q7'		100	52	ns
f_{max}	maximum clock frequency SH_CP and ST_CP		100	57	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	115	130	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts;
   N = total load switching outputs;
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. For 74HC595 the condition is V_I = GND to V_{CC}.
   For 74HCT595 the condition is V_I = GND to V_{CC} − 1.5 V.

FUNCTION TABLE

See note 1.

INPUT					OUTPUT		FUNCTION
SH_CP	ST_CP	$\overline{OE}$	$\overline{MR}$	DS	Q7’	Qn	
X	X	L	L	X	L	n.c.	a LOW level on $\overline{MR}$ only affects the shift registers
X	↑	L	L	X	L	L	empty shift register loaded into storage register
X	X	H	L	X	L	Z	shift register clear; parallel outputs in high-impedance OFF-state
↑	X	L	H	H	Q6’	n.c.	logic high level shifted into shift register stage 0; contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6’) appears on the serial output (Q7’)
X	↑	L	H	X	n.c.	Qn’	contents of shift register stages (internal Qn’) are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Q6’	Qn’	contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages

Note

1. H = HIGH voltage level;
   L = LOW voltage level;
   ↑ = LOW-to-HIGH transition;
   ↓ = HIGH-to-LOW transition;
   Z = high-impedance OFF-state;
   n.c. = no change;
   X = don’t care.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74HC595N	–40 to +125 °C	16	DIP16	plastic	SOT38-4
74HCT595N	–40 to +125 °C	16	DIP16	plastic	SOT38-4
74HC595D	–40 to +125 °C	16	SO16	plastic	SOT109-1
74HCT595D	–40 to +125 °C	16	SO16	plastic	SOT109-1
74HC595DB	–40 to +125 °C	16	SSOP16	plastic	SOT338-1
74HCT595DB	–40 to +125 °C	16	SSOP16	plastic	SOT338-1
74HC595PW	–40 to +125 °C	16	TSSOP16	plastic	SOT403-1
74HCT595PW	–40 to +125 °C	16	TSSOP16	plastic	SOT403-1
74HC595BQ	–40 to +125 °C	16	DHVQFN16	plastic	SOT763-1
74HCT595BQ	–40 to +125 °C	16	DHVQFN16	plastic	SOT763-1

PINNING

PIN	SYMBOL	DESCRIPTION
1	Q1	parallel data output
2	Q2	parallel data output
3	Q3	parallel data output
4	Q4	parallel data output
5	Q5	parallel data output
6	Q6	parallel data output
7	Q7	parallel data output
8	GND	ground (0 V)
9	Q7’	serial data output
10	$\overline{MR}$	master reset (active LOW)
11	SH_CP	shift register clock input
12	ST_CP	storage register clock input
13	$\overline{OE}$	output enable (active LOW)
14	DS	serial data input
15	Q0	parallel data output
16	V_{CC}	positive supply voltage

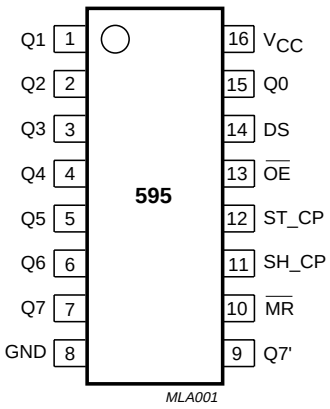
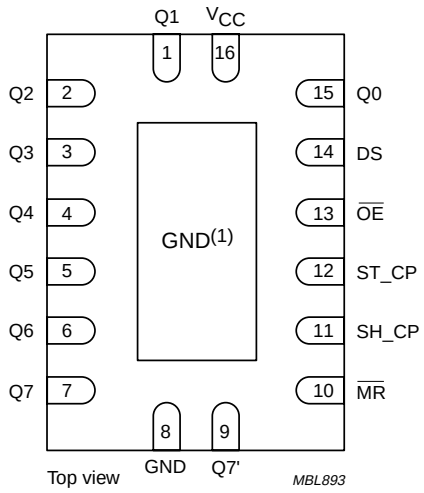


Fig.1 Pin configuration DIP16, SO16 and (T)SSOP16.



(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig.2 Pin configuration DHVQFN16.

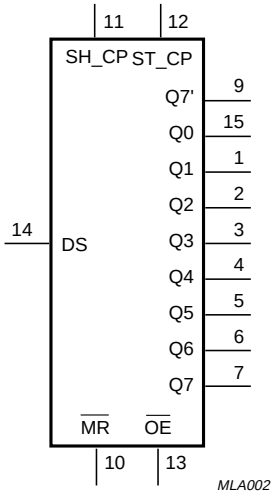


Fig.3 Logic symbol.

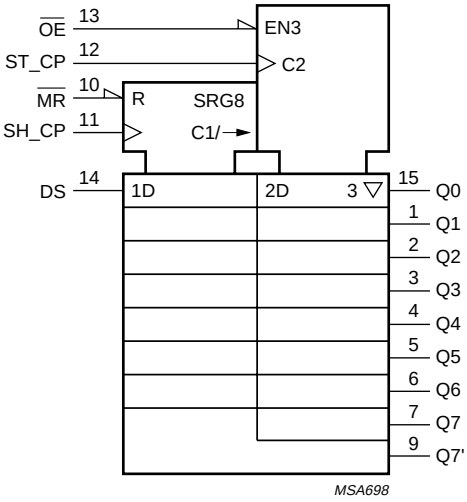


Fig.4 IEC logic symbol.

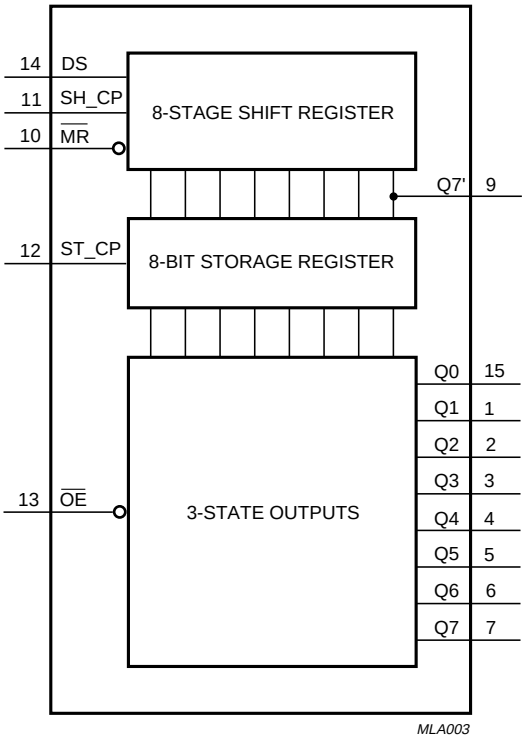


Fig.5 Functional diagram.

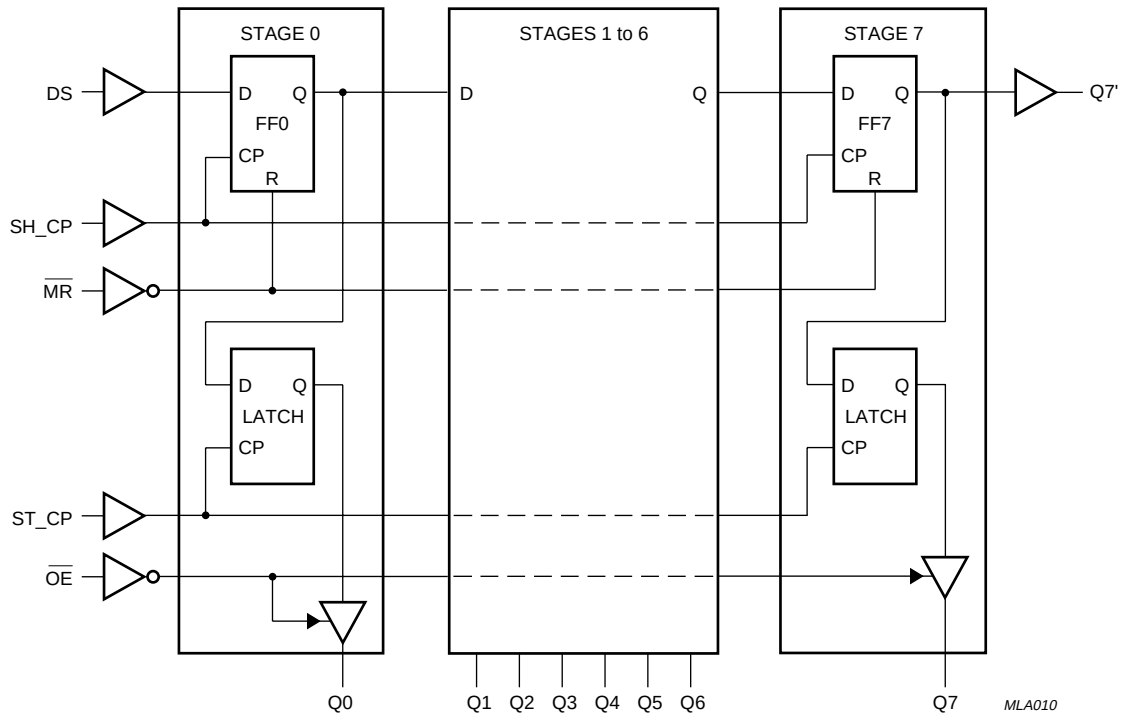


Fig.6 Logic diagram.

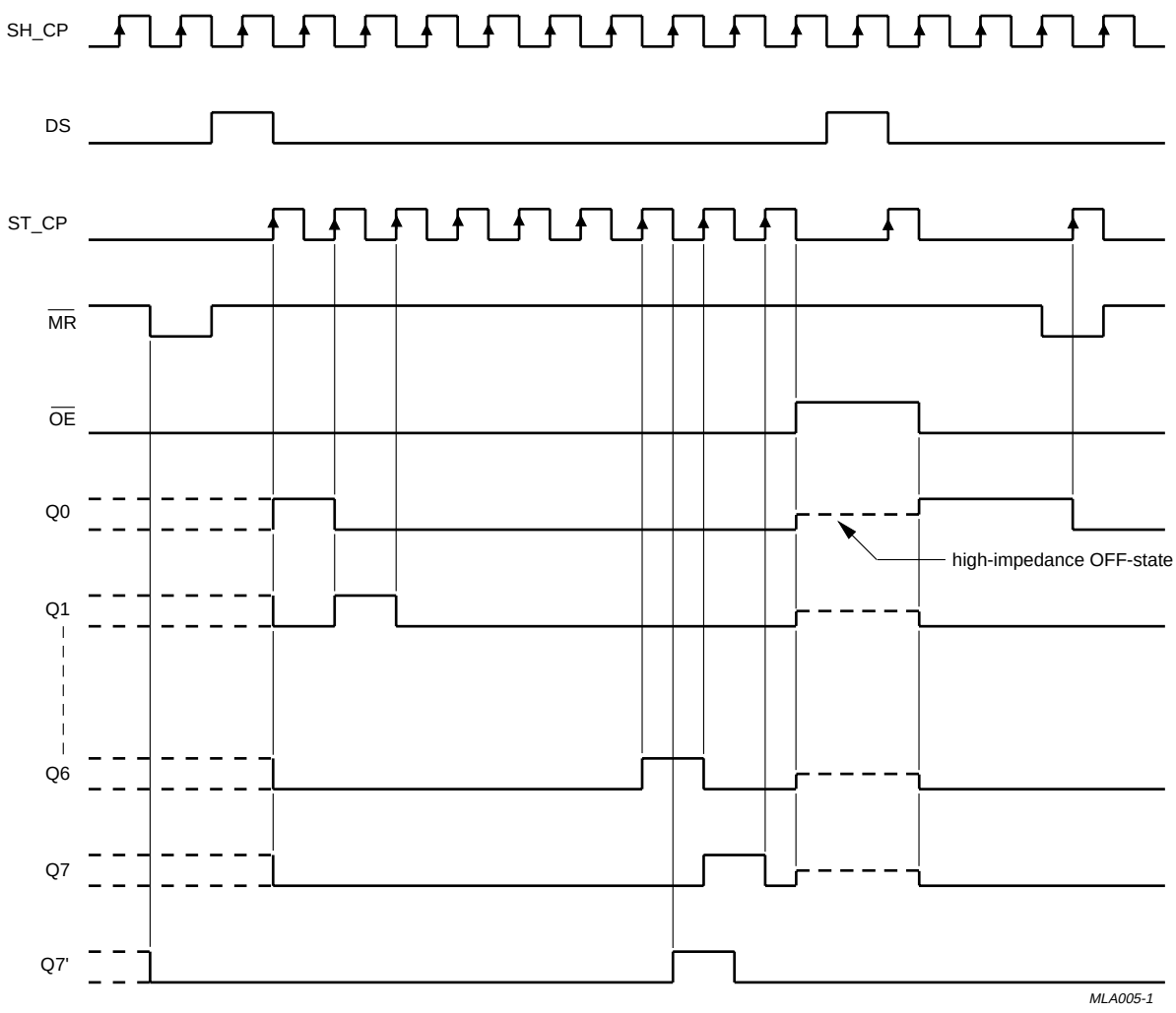


Fig.6 Timing diagram.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74HC			74HCT			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	–	V_{CC}	0	–	V_{CC}	V
V_O	output voltage		0	–	V_{CC}	0	–	V_{CC}	V
T_{amb}	ambient temperature		–40	–	+125	–40	–	+125	°C
t_r, t_f	input rise and fall time	V_{CC} = 2.0 V	–	–	1000	–	–	–	ns
		V_{CC} = 4.5 V	–	6.0	500	–	6.0	500	ns
		V_{CC} = 6.0 V	–	–	400	–	–	–	ns

LIMITED VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+7.0	V
I_{IK}	input diode current	V_I < –0.5 V to V_I > V_{CC} + 0.5 V	–	±20	mA
I_{OK}	output diode current	V_O < –0.5 V to V_O > V_{CC} + 0.5 V	–	±20	mA
I_O	output source or sink current	V_O = –0.5 V to V_{CC} + 0.5 V			
		Q7’ standard output	–	±25	mA
		Qn bus driver outputs	–	±35	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±70	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 to +125 °C; note 1	–	500	mW

Note

1. For DIP16 packages: above 70 °C derate linearly with 12 mW/K.
   For SO16 packages: above 70 °C derate linearly with 8 mW/K.
   For SSOP16 packages: above 60 °C derate linearly with 5.5 mW/K.
   For TSSOP16 packages: above 60 °C derate linearly with 5.5 mW/K.
   For DHVQFN16 packages: above 60 °C derate linearly with 4.5 mW/K.

DC CHARACTERISTICS

Type 74HC

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to +85 °C; note 1							
V_{IH}	HIGH-level input voltage		2.0	1.5	1.2	–	V
			4.5	3.15	2.4	–	V
			6.0	4.2	3.2	–	V
V_{IL}	LOW-level input voltage		2.0	–	0.8	0.5	V
			4.5	–	2.1	1.35	V
			6.0	–	2.8	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		all outputs					
		I_O = –20 μA	2.0	1.9	2.0	–	V
			4.5	4.4	4.5	–	V
			6.0	5.9	6.0	–	V
		Q7’ standard output					
		I_O = –4.0 mA	4.5	3.84	4.32	–	V
		I_O = –5.2 mA	6.0	5.34	5.81	–	V
		Qn bus driver outputs					
		I_O = –6.0 mA	4.5	3.84	4.32	–	V
		I_O = –7.8 mA	6.0	5.34	5.81	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		all outputs					
		I_O = 20 μA	2.0	–	0	0.1	V
			4.5	–	0	0.1	V
			6.0	–	0	0.1	V
		Q7’ standard output					
		I_O = 4.0 mA	4.5	–	0.15	0.33	V
		I_O = 5.2 mA	6.0	–	0.16	0.33	V
		Qn bus driver outputs					
		I_O = 6.0 mA	4.5	–	0.16	0.33	V
		I_O = 7.8 mA	6.0	–	0.16	0.33	V
I_{LI}	input leakage current	V_I = V_{CC} or GND	6.0	–	–	±1.0	μA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND	6.0	–	–	±5.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	6.0	–	–	80	μA

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to +125 °C							
V_{IH}	HIGH-level input voltage		2.0	1.5	–	–	V
			4.5	3.15	–	–	V
			6.0	4.2	–	–	V
V_{IL}	LOW-level input voltage		2.0	–	–	0.5	V
			4.5	–	–	1.35	V
			6.0	–	–	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		all outputs					
		I_O = −20 μA	2.0	1.9	–	–	V
			4.5	4.4	–	–	V
			6.0	5.9	–	–	V
		Q7’ standard output					
		I_O = −4.0 mA	4.5	3.7	–	–	V
		I_O = −5.2 mA	6.0	5.2	–	–	V
		Qn bus driver outputs					
		I_O = −6.0 mA	4.5	3.7	–	–	V
		I_O = −7.8 mA	6.0	5.2	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		all outputs					
		I_O = 20 μA	4.5	–	–	0.1	V
		Q7’ standard output					
		I_O = 4.0 mA	4.5	–	–	0.4	V
		Qn bus driver outputs					
		I_O = 6.0 mA	4.5	–	–	0.4	V
I_{LI}	input leakage current	V_I = V_{CC} or GND	5.5	–	–	±1.0	μA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND	5.5	–	–	±10.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	5.5	–	–	160	μA

Note

1. All typical values are measured at T_{amb} = 25 °C.

Type 74HCT

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $t_r = t_f$ = 6 ns; C_L = 50 pF.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to +85 °C; note 1							
V_{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	1.6	–	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	–	1.2	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		all outputs I_O = −20 μA	4.5	4.4	4.5	–	V
		Q7' standard output I_O = −4.0 mA	4.5	3.84	4.32	–	V
		Qn bus driver outputs I_O = −6.0 mA	4.5	3.7	4.32	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		all outputs I_O = 20 μA	4.5	–	0	0.33	V
		Q7' standard output I_O = 4.0 mA	4.5	–	0.15	0.33	V
		Qn bus driver outputs I_O = 6.0 mA	4.5	–	0.16	0.33	V
I_{LI}	input leakage current	V_I = V_{CC} or GND	5.5	–	–	±1.0	μA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND	5.5	–	–	±5.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	5.5	–	–	80	μA
ΔI_{CC}	additional supply current per input	V_I = V_{CC} − 2.1 V; I_O = 0; note 2	4.5 to 5.5	–	100	450	μA

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to +125 °C							
V_{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		all outputs I_O = −20 μA	4.5	4.4	–	–	V
		Q7' standard output I_O = −4.0 mA	4.5	3.7	–	–	V
		Qn bus driver outputs I_O = −6.0 mA	4.5	3.7	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		all outputs I_O = 20 μA	4.5	–	–	0.1	V
		Q7' standard output I_O = 4.0 mA	4.5	–	–	0.4	V
		Qn bus driver outputs I_O = 6.0 mA	4.5	–	–	0.4	V
I_{LI}	input leakage current	V_I = V_{CC} or GND	5.5	–	–	±1.0	μA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND	5.5	–	–	±10.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	5.5	–	–	160	μA
ΔI_{CC}	additional supply current per input	V_I = V_{CC} − 2.1 V; I_O = 0; note 2	4.5 to 5.5	–	–	490	μA

Notes

1. All typical values are measured at T_{amb} = 25 °C.
2. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient per input pin:
   a. pin DS: 0.25
   b. pins $\overline{MR}$, SH_CP, ST_CP and $\overline{OE}$: 1.50.

AC CHARACTERISTICS

Family 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = 25 °C							
t_{PHL}/t_{PLH}	propagation delay SH_CP to Q7'	see Fig.7	2.0	–	52	160	ns
			4.5	–	19	32	ns
			6.0	–	15	27	ns
	propagation delay ST_CP to Qn	see Fig.8	2.0	–	55	175	ns
			4.5	–	20	35	ns
			6.0	–	16	30	ns
t_{PHL}	propagation delay $\overline{MR}$ to Q7'	see Fig.10	2.0	–	47	175	ns
			4.5	–	17	35	ns
			6.0	–	14	30	ns
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Qn	see Fig.11	2.0	–	47	150	ns
			4.5	–	17	30	ns
			6.0	–	14	26	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Qn	see Fig.11	2.0	–	41	150	ns
			4.5	–	15	30	ns
			6.0	–	12	26	ns
t_W	shift clock pulse width HIGH or LOW	see Fig.7	2.0	75	17	–	ns
			4.5	15	6	–	ns
			6.0	13	5	–	ns
	storage clock pulse width HIGH or LOW	see Fig.8	2.0	75	11	–	ns
			4.5	15	4	–	ns
			6.0	13	3	–	ns
	master reset pulse width LOW	see Fig.10	2.0	75	17	–	ns
			4.5	15	6.0	–	ns
			6.0	13	5.0	–	ns
t_{su}	set-up time DS to SH_CP	see Fig.9	2.0	50	11	–	ns
			4.5	10	4.0	–	ns
			6.0	9.0	3.0	–	ns
	set-up time SH_CP to ST_CP	see Fig.8	2.0	75	22	–	ns
			4.5	15	8	–	ns
			6.0	13	7	–	ns
t_h	hold time DS to SH_CP	see Fig.9	2.0	+3	–6	–	ns
			4.5	+3	–2	–	ns
			6.0	+3	–2	–	ns

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
t_{rem}	removal time $\overline{MR}$ to SH_CP	see Fig.10	2.0	+50	–19	–	ns
			4.5	+10	–7	–	ns
			6.0	+9	–6	–	ns
f_{max}	maximum clock pulse frequency SH_CP or ST_CP	see Figs 7 and 8	2.0	9	30	–	MHz
			4.5	30	91	–	MHz
			6.0	35	108	–	MHz
T_{amb} = –40 to +85 °C							
t_{PHL}/t_{PLH}	propagation delay SH_CP to Q7’	see Fig.7	2.0	–	–	200	ns
			4.5	–	–	40	ns
			6.0	–	–	34	ns
	propagation delay ST_CP to An	see Fig.8	2.0	–	–	220	ns
			4.5	–	–	44	ns
			6.0	–	–	37	ns
t_{PHL}	propagation delay $\overline{MR}$ to Q7’	see Fig.10	2.0	–	–	220	ns
			4.5	–	–	44	ns
			6.0	–	–	37	ns
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Qn	see Fig.11	2.0	–	–	190	ns
			4.5	–	–	38	ns
			6.0	–	–	33	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Qn	see Fig.11	2.0	–	–	190	ns
			4.5	–	–	38	ns
			6.0	–	–	33	ns
t_W	shift clock pulse width HIGH or LOW	see Fig.7	2.0	95	–	–	ns
			4.5	19	–	–	ns
			6.0	16	–	–	ns
	storage clock pulse width HIGH or LOW	see Fig.8	2.0	95	–	–	ns
			4.5	19	–	–	ns
			6.0	16	–	–	ns
	master reset pulse width LOW	see Fig.10	2.0	95	–	–	ns
			4.5	19	–	–	ns
			6.0	16	–	–	ns
t_{su}	set-up time DS to SH_CP	see Fig.9	2.0	65	–	–	ns
			4.5	13	–	–	ns
			6.0	11	–	–	ns
	set-up time SH_CP to ST_CP	see Fig.8	2.0	95	–	–	ns
			4.5	19	–	–	ns
			6.0	16	–	–	ns

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
t_h	hold time DS to SH_CP	see Fig.9	2.0	3	–	–	ns
			4.5	3	–	–	ns
			6.0	3	–	–	ns
t_{rem}	removal time $\overline{MR}$ to SH_CP	see Fig.10	2.0	65	–	–	ns
			4.5	13	–	–	ns
			6.0	11	–	–	ns
f_{max}	maximum clock pulse frequency SH_CP or ST_CP	see Figs 7 and 8	2.0	4.8	–	–	MHz
			4.5	24	–	–	MHz
			6.0	28	–	–	MHz
T_{amb} = −40 to +125 °C							
t_{PHL}/t_{PLH}	propagation delay SH_CP to Q7’	see Fig.7	2.0	–	–	240	ns
			4.5	–	–	48	ns
			6.0	–	–	41	ns
	propagation delay ST_CP to Qn	see Fig.8	2.0	–	–	265	ns
			4.5	–	–	53	ns
			6.0	–	–	45	ns
t_{PHL}	propagation delay $\overline{MR}$ to Q7’	see Fig.10	2.0	–	–	265	ns
			4.5	–	–	53	ns
			6.0	–	–	45	ns
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Qn	see Fig.11	2.0	–	–	225	ns
			4.5	–	–	45	ns
			6.0	–	–	38	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Qn	see Fig.11	2.0	–	–	225	ns
			4.5	–	–	45	ns
			6.0	–	–	38	ns
t_W	shift clock pulse width HIGH or LOW	see Fig.7	2.0	110	–	–	ns
			4.5	22	–	–	ns
			6.0	19	–	–	ns
	storage clock pulse width HIGH or LOW	see Fig.8	2.0	110	–	–	ns
			4.5	22	–	–	ns
			6.0	19	–	–	ns
	master reset pulse width LOW	see Fig.10	2.0	110	–	–	ns
			4.5	22	–	–	ns
			6.0	19	–	–	ns

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
t_{su}	set-up time DS to SH_CP	see Fig.9	2.0	75	–	–	ns
			4.5	15	–	–	ns
			6.0	13	–	–	ns
	set-up time SH_CP to ST_CP	see Fig.8	2.0	110	–	–	ns
			4.5	22	–	–	ns
			6.0	19	–	–	ns
t_h	hold time DS to SH_CP	see Fig.9	2.0	3	–	–	ns
			4.5	3	–	–	ns
			6.0	3	–	–	ns
t_{rem}	removal time $\overline{MR}$ to SH_CP	see Fig.10	2.0	75	–	–	ns
			4.5	15	–	–	ns
			6.0	13	–	–	ns
f_{max}	maximum clock pulse frequency SH_CP or ST_CP	see Figs 7 and 8	2.0	4	–	–	MHz
			4.5	20	–	–	MHz
			6.0	24	–	–	MHz

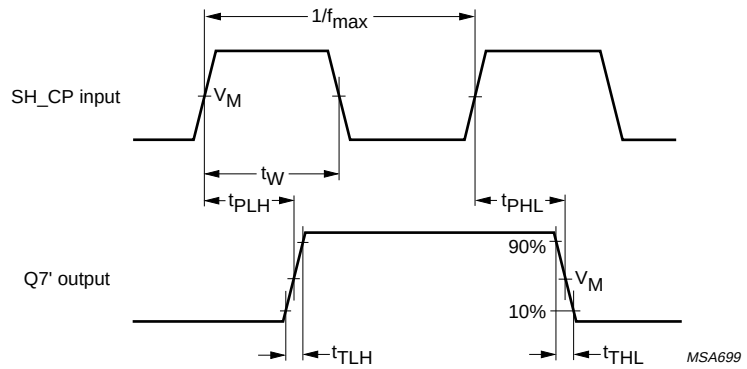
Family 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = 25 °C							
t_{PHL}/t_{PLH}	propagation delay SH_CP to Q7'	see Fig.7	4.5	–	25	42	ns
	propagation delay ST_CP to Qn	see Fig.8	4.5	–	24	40	ns
t_{PHL}	propagation delay $\overline{MR}$ to Q7'	see Fig.10	4.5	–	23	40	ns
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Qn	see Fig.11	4.5	–	21	35	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Qn	see Fig.11	4.5	–	18	30	ns
t_W	shift clock pulse width HIGH or LOW	see Fig.7	4.5	16	6	–	ns
	storage clock pulse width HIGH or LOW	see Fig.8	4.5	16	5	–	ns
	master reset pulse width LOW	see Fig.10	4.5	20	8	–	ns
t_{su}	set-up time DS to SH_CP	see Fig.9	4.5	16	5	–	ns
	set-up time SH_CP to ST_CP	see Fig.8	4.5	16	8	–	ns
t_h	hold time DS to SH_CP	see Fig.9	4.5	+3	–2	–	ns
t_{rem}	removal time $\overline{MR}$ to SH_CP	see Fig.10	4.5	+10	–7	–	ns
f_{max}	maximum clock pulse frequency SH_CP or ST_CP	see Figs 7 and 8	4.5	30	52	–	MHz
T_{amb} = −40 to +85 °C							
t_{PHL}/t_{PLH}	propagation delay SH_CP to Q7'	see Fig.7	4.5	–	–	53	ns
	propagation delay ST_CP to Qn	see Fig.8	4.5	–	–	50	ns
t_{PHL}	propagation delay $\overline{MR}$ to Q7'	see Fig.10	4.5	–	–	50	ns
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Qn	see Fig.11	4.5	–	–	44	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Qn	see Fig.11	4.5	–	–	38	ns

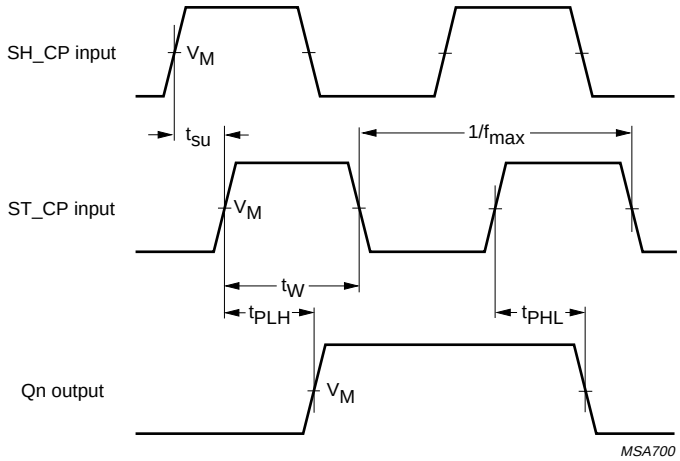
SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
t_W	shift clock pulse width HIGH or LOW	see Fig.7	4.5	20	–	–	ns
	storage clock pulse width HIGH or LOW	see Fig.8	4.5	20	–	–	ns
	master reset pulse width LOW	see Fig.10	4.5	25	–	–	ns
t_{su}	set-up time DS to SH_CP	see Fig.9	4.5	20	–	–	ns
	set-up time SH_CP to ST_CP	see Fig.8	4.5	20	–	–	ns
t_h	hold time DS to SH_CP	see Fig.9	4.5	3	–	–	ns
t_{rem}	removal time $\overline{MR}$ to SH_CP	see Fig.10	4.5	13	–	–	ns
f_{max}	maximum clock pulse frequency SH_CP or ST_CP	see Figs 7 and 8	4.5	24	–	–	MHz
T_{amb} = −40 to +125 °C							
t_{PHL}/t_{PLH}	propagation delay SH_CP to Q7’	see Fig.7	4.5	–	–	63	ns
	propagation delay ST_CP to Qn	see Fig.8	4.5	–	–	60	ns
t_{PHL}	propagation delay $\overline{MR}$ to Q7’	see Fig.10	4.5	–	–	60	ns
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Qn	see Fig.11	4.5	–	–	53	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Qn	see Fig.11	4.5	–	–	45	ns
t_W	shift clock pulse width HIGH or LOW	see Fig.7	4.5	24	–	–	ns
	storage clock pulse width HIGH or LOW	see Fig.8	4.5	24	–	–	ns
	master reset pulse width LOW	see Fig.10	4.5	30	–	–	ns
t_{su}	set-up time DS to SH_CP	see Fig.9	4.5	24	–	–	ns
	set-up time SH_CP to ST_CP	see Fig.8	4.5	24	–	–	ns
t_h	hold time DS to SH_CP	see Fig.9	4.5	3	–	–	ns
t_{rem}	removal time $\overline{MR}$ to SH_CP	see Fig.10	4.5	15	–	–	ns
f_{max}	maximum clock pulse frequency SH_CP or ST_CP	see Figs 7 and 8	4.5	20	–	–	MHz

AC WAVEFORMS



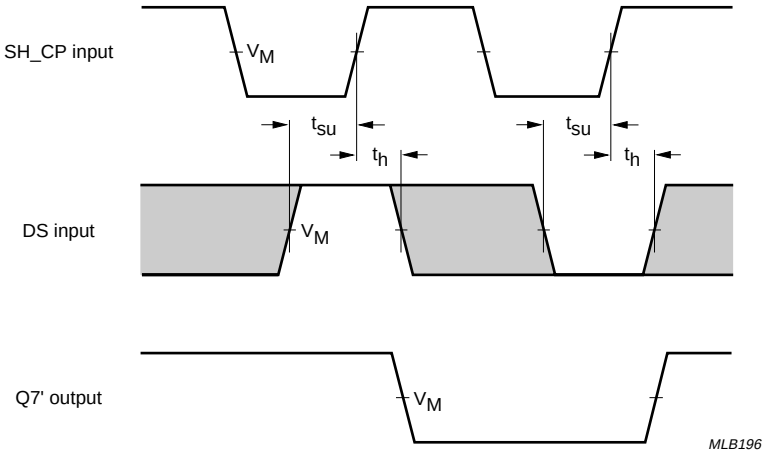
74HC595: V_M = 50%; V_I = GND to V_{CC}.
74HCT595: V_M = 1.3 V; V_I = GND to 3 V.

Fig.7 Waveforms showing the clock (SH_CP) to output (Q7') propagation delays, the shift clock pulse width and maximum shift clock frequency.



74HC595: V_M = 50%; V_I = GND to V_{CC}.
74HCT595: V_M = 1.3 V; V_I = GND to 3 V.

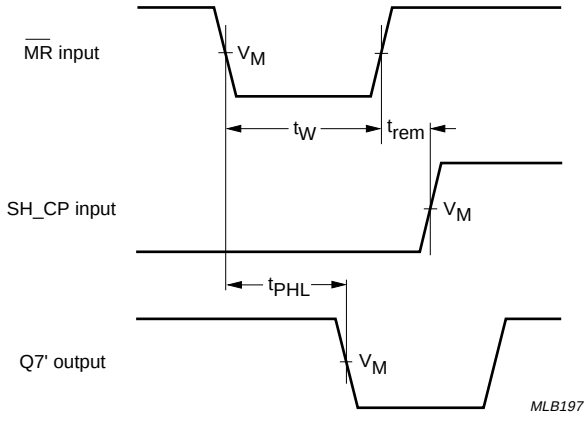
Fig.8 Waveforms showing the storage clock (ST_CP) to output (Qn) propagation delays, the storage clock pulse width and the shift clock to storage clock set-up time.



74HC595: V_M = 50%; V_I = GND to V_{CC}.
74HCT595: V_M = 1.3 V; V_I = GND to 3 V.

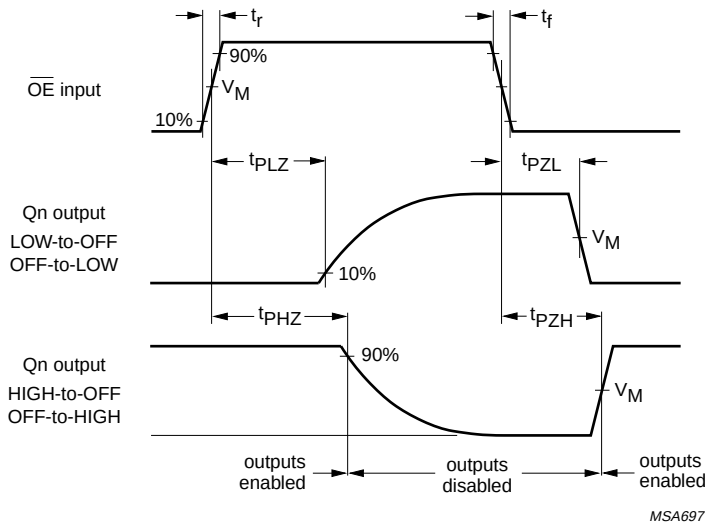
The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig.9 Waveforms showing the data set-up and hold times for the DS input.



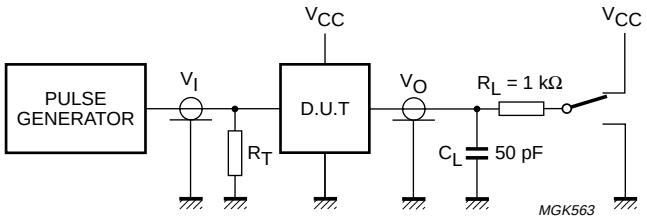
74HC595: V_M = 50%; V_I = GND to V_{CC}.
74HCT595: V_M = 1.3 V; V_I = GND to 3 V.

Fig.10 Waveforms showing the Master Reset ($\overline{MR}$) pulse width, the master reset to output (Q7') propagation delay and the master reset to shift clock (SH_CP) removal time.



74HC595: V_M = 50%; V_I = GND to V_{CC}.
74HCT595: V_M = 1.3 V; V_I = GND to 3 V.

Fig.11 Waveforms showing the 3-state enable and disable times for input $\overline{OE}$.



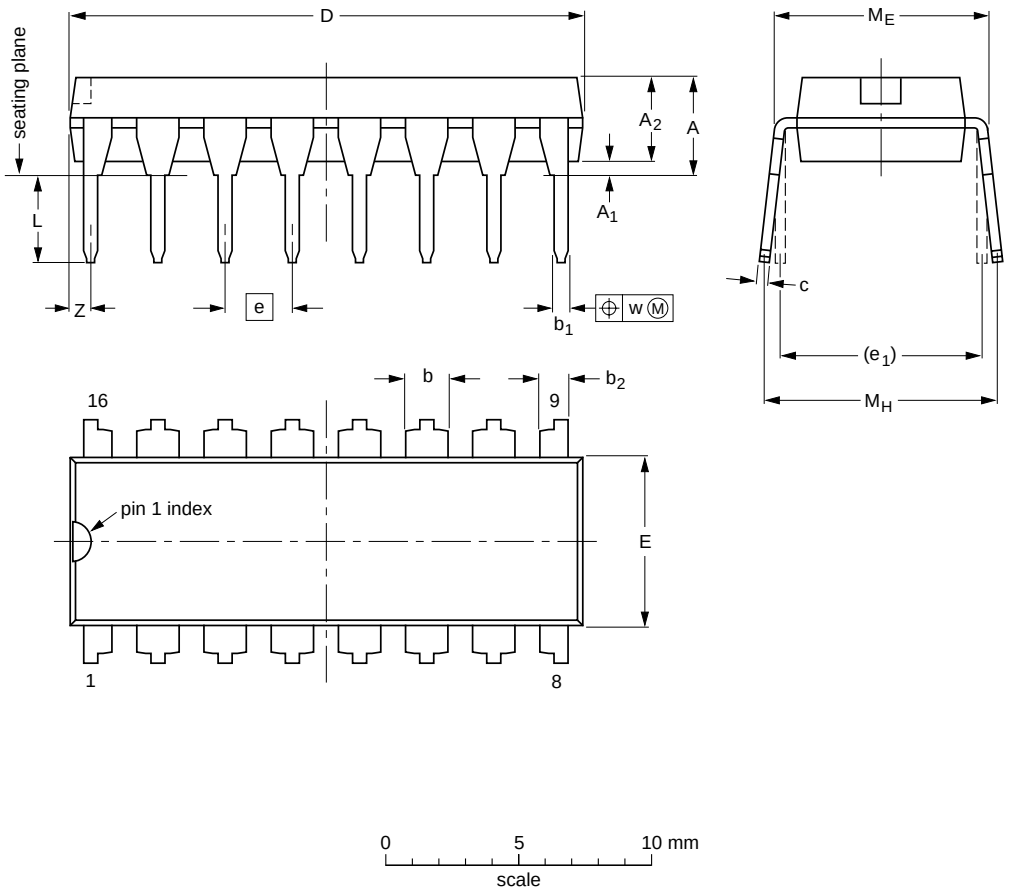
TEST	SWITCH
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

Definitions for test circuit:
R_L = Load resistor.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.12 Test circuit for 3-state outputs.

PACKAGE OUTLINES

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

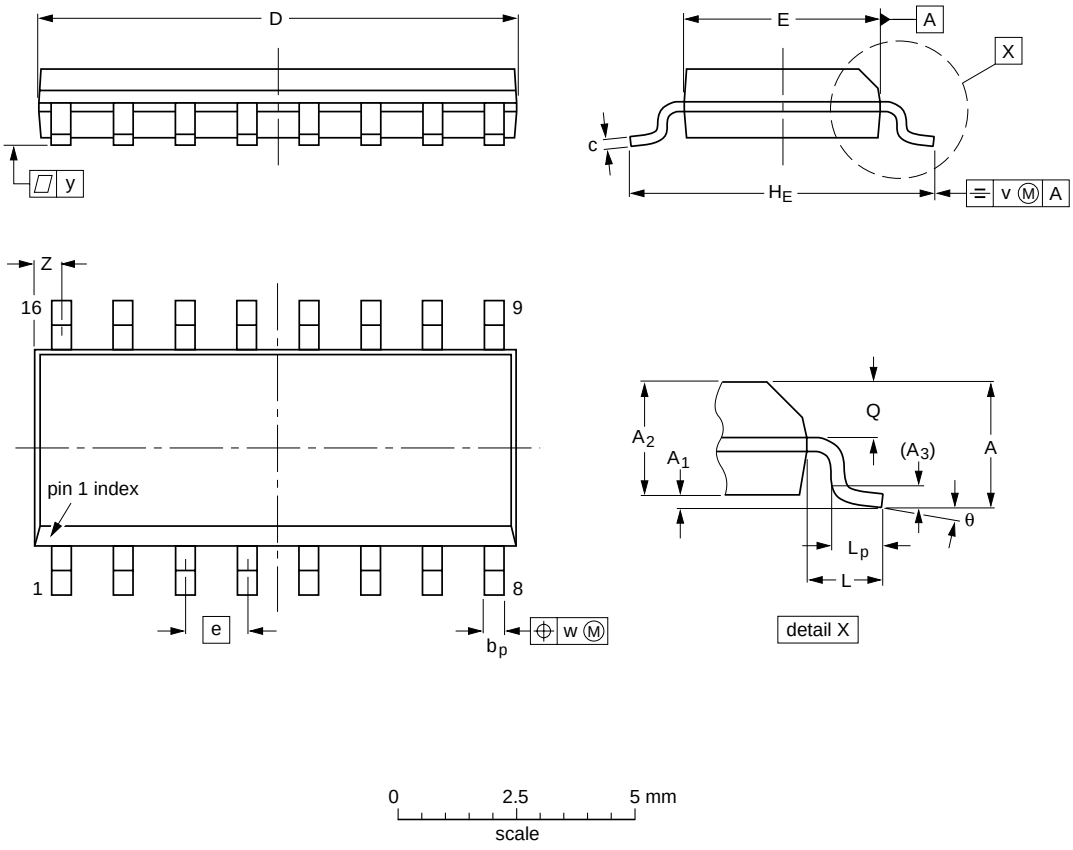
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						~~95-01-14~~ 03-02-13

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

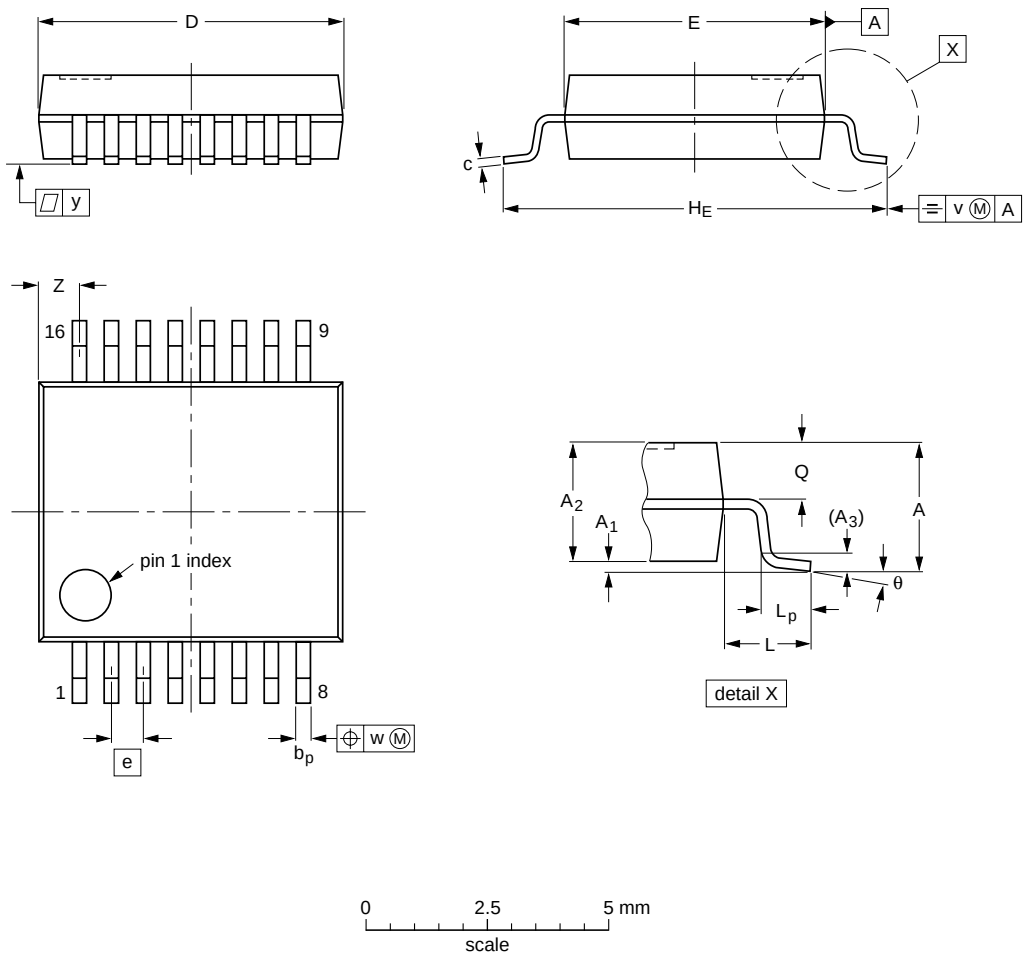
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

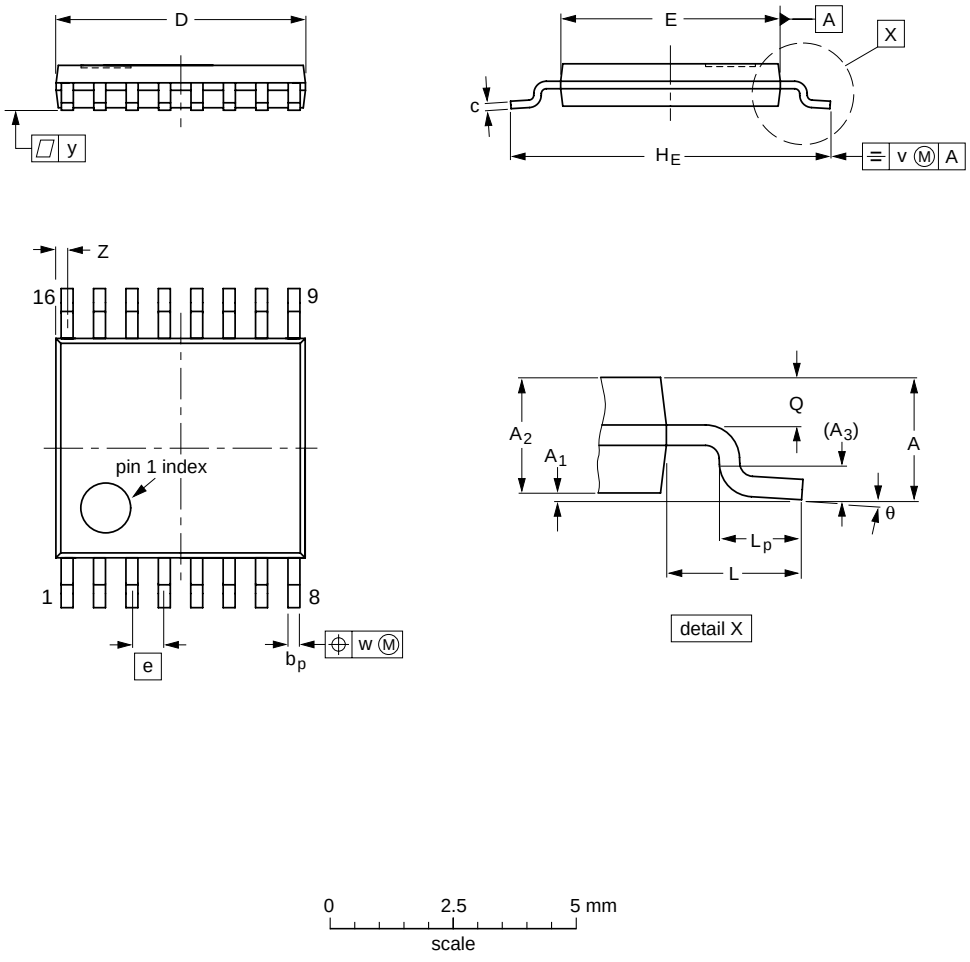
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

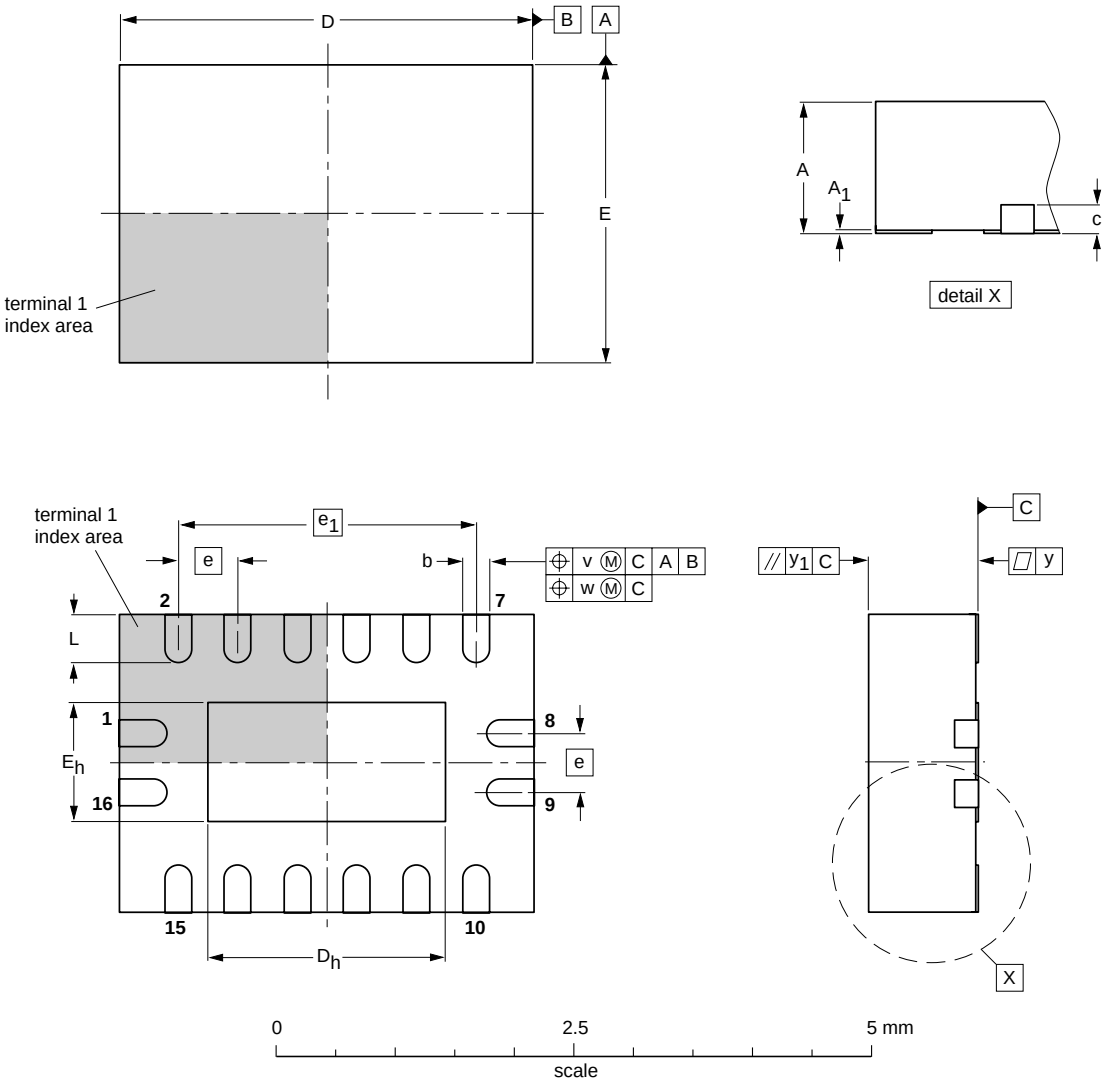
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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